REMARKS/ARGUMENTS

Claims 1, 3, 5-8, 10, 12-21, 23, 25-32, 34-37 are now pending in this application. Claims 1, 3, 5, 12-16, 20-21, 23, 25, 31-32 and 34 are amended. Claims 9, 24 and 33 are cancelled. Claims 1, 12, 13, 20, 21 and 31 are the only independent claims.

Claim Objections

The objection to claim 24 is moot as claim 24 is cancelled.

Support for Amendments

Support for the amendments is found in, for instance, Figure 1B and Figure 3, and in the specification as filed at, for instance, page 4, lines 16 – page 9, line 9.

Claim Rejections – 35 USC § 103

The Office Action rejected claims 1, 3, 5-10 and 12 -37 under 35 USC 103 (a) as being unpatentable over Stevens (US 6,173,345) and one of ordinary skill in the art.

Stevens teaches a method of levelizing data transfer delays between a set of system devices and a bus controller, meaning that the data transfer delay is adjusted so that the sum of the data transfer delay and the propagation delay is equal to the same number of bus cycles for all devices on the bus so that the bus controller can respond to the entire set of system devices in a uniform manner (Steven, Column 1, lines 26-34).

The method Stevens teaches determines the largest transfer latency from a device to the controller and sets all the delays to be that largest amount. The delay determined by Stevens is a one way delay.

Stephens teaches introducing the data delay using delay registers (column 1, lines 62 – column 2 lines 4). This results in delays that can be added in as integer values of the bus cycle or clock time.

The data used in Steven to determine the one-way delay is not pre-determined in the sense of it being known in advance by the memory device. Instead, it is data that is written into the memory and then retrieved.

In contrast, applicant's invention, in the embodiment of claim 1, addresses a data skew problem. In particular, applicant's invention overcomes a round trip timing delay problem of a communications system in which two devices both use a framing signal and a clocking signal transmitted from one device. This causes an incoming signal to the clock transmitting device to be offset from the clocking signal by the roundtrip

communications delay between the two devices. For optimal communications, this round-trip delay needs to be determined and compensated for.

Applicant's invention of claim 1 includes an initialization procedure that measures and compensates for the round-trip delay using a suitable test bit pattern that is known in advance by both devices.

In one embodiment of applicant's invention, the initialization includes having the device that is transmitting the clocking signal transmit an instruction to start to the first device. This is an instruction to transmit the predetermined bit pattern at the start of the next frame signal. After receiving the instruction to start, the first device transmits the predetermined bit pattern, using the clock signal and the framing signal transmitted by the second device. The second device then samples the received signal on the leading or falling edges of the clock signal. The sampling begins a delay period after the second device sent the start signal. If the second device does not detect the correct pattern, the process is repeated, but the delay period is extended by a fraction of a clock period, typically half a clock period. This process is repeated until the second device detects the correct signal. The first delay period that results in correct reception of the pre-determined bit-pattern is then used as the delay for the remainder of the communications session.

To further emphasize the differences between the cited prior art and applicant's invention embodied in claim 1, claim 1 is amended to now recite:

> 1. (currently amended) A method of digital communication between two devices, said method comprising the steps of:
>
> (1) a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;
>
> (2) said second device sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal ~~as a function of~~ beginning a delay period after said start signal;
>
> (3) if said second device does not detect said predetermined bit pattern, increasing said delay period by a fraction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

(4) if said second device detects said predetermined bit pattern, setting the last delay period used in step (2) as a delay period to be used by said second device for sampling data for further transmissions from said first device to said second device;

(5) said second device using said last delay period for sampling all further data transmissions from said first device to said second device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

The Office Action does not show where Stevens teaches:

a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;

or

(3) if said second device does not detect said predetermined bit pattern, increasing said delay period by a fraction of a clock period and repeating steps (1) and (2), and, if necessary, step (3);

Stevens teaches re-reading data written into a memory. Only the one-way delay from the memory to the controller is measured in this way, which would not necessarily provide the round-trip delay because of possible asymmetries in the communications system.

Stevens teaches incrementing delays using storage registers. This results in delays that are integers of a full clock cycle. As detailed on page 16, lines 8 – 20, delays that are a clock cycle or longer make it possible to miss the correct sampling point in a round trip communications situations.

As the Office Action does not show where Stevens teaches all the elements of claim 1 or explain how they would be obvious to one of ordinary skill in the art, the Office Action does not show how independent claims 1, 12, 13, 20, 21 and 31 are

obvious. Applicant, therefore, requests that the rejection be withdrawn and claims 1, 12, 13, 20, 21 and 31 allowed.

As dependent claims 3, 5-8, 10, 13-19, 23, 25-30, 32 and 34-37 now depend from, and include all the limitations, of allowable claims, they too are allowable. Applicant, therefore, requests that the rejection be withdrawn and claims 3, 5-8, 10, 13-19, 23, 25-30, 32 and 34-37 allowed.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant believes claims 1, 3, 5-8, 10, 12-21, 23, 25-32, 34-37 to be patentable and the application to be in condition for allowance, and respectfully requests issuance of a Notice of Allowance. If any issues remain, the undersigned requests a telephone interview prior to the issuance of an action.

Respectfully Submitted,

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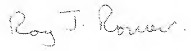

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